

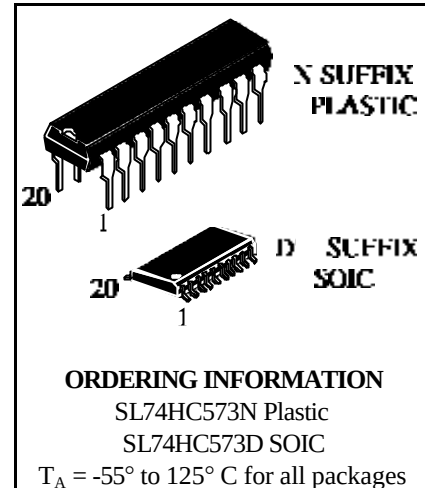
# Octal 3-State Noninverting Transparent Latch

## High-Performance Silicon-Gate CMOS

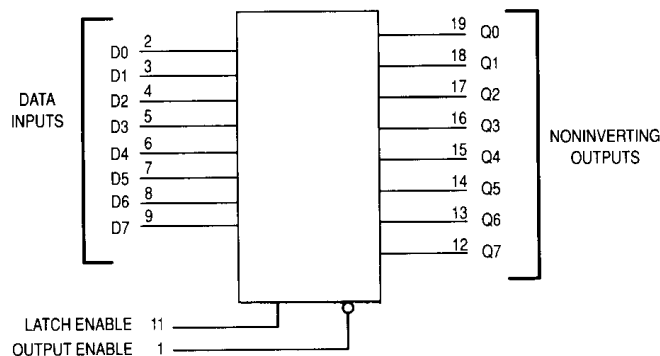
The SL74HC573 is identical in pinout to the LS/ALS573. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



## LOGIC DIAGRAM



## PIN ASSIGNMENT

|               |    |    |              |
|---------------|----|----|--------------|
| OUTPUT ENABLE | 1  | 20 | $V_{CC}$     |
| D0            | 2  | 19 | Q0           |
| D1            | 3  | 18 | Q1           |
| D2            | 4  | 17 | Q2           |
| D3            | 5  | 16 | Q3           |
| D4            | 6  | 15 | Q4           |
| D5            | 7  | 14 | Q5           |
| D6            | 8  | 13 | Q6           |
| D7            | 9  | 12 | Q7           |
| GND           | 10 | 11 | LATCH ENABLE |

## FUNCTION TABLE

| Inputs        |              |   | Output    |
|---------------|--------------|---|-----------|
| Output Enable | Latch Enable | D | Q         |
| L             | H            | H | H         |
| L             | H            | L | L         |
| L             | L            | X | no change |
| H             | X            | X | Z         |

X = don't care

Z = high impedance

## MAXIMUM RATINGS\*

| Symbol           | Parameter                                                                        | Value                        | Unit |
|------------------|----------------------------------------------------------------------------------|------------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage (Referenced to GND)                                            | -0.5 to +7.0                 | V    |
| V <sub>IN</sub>  | DC Input Voltage (Referenced to GND)                                             | -1.5 to V <sub>CC</sub> +1.5 | V    |
| V <sub>OUT</sub> | DC Output Voltage (Referenced to GND)                                            | -0.5 to V <sub>CC</sub> +0.5 | V    |
| I <sub>IN</sub>  | DC Input Current, per Pin                                                        | ±20                          | mA   |
| I <sub>OUT</sub> | DC Output Current, per Pin                                                       | ±35                          | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                                  | ±75                          | mA   |
| P <sub>D</sub>   | Power Dissipation in Still Air, Plastic DIP+<br>SOIC Package+                    | 750<br>500                   | mW   |
| T <sub>stg</sub> | Storage Temperature                                                              | -65 to +150                  | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260                          | °C   |

\*Maximum Ratings are those values beyond which damage to the device may occur.  
Functional operation should be restricted to the Recommended Operating Conditions.  
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter                                                                                                            | Min         | Max                | Unit |
|------------------------------------|----------------------------------------------------------------------------------------------------------------------|-------------|--------------------|------|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                                                                                | 2.0         | 6.0                | V    |
| V <sub>IN</sub> , V <sub>OUT</sub> | DC Input Voltage, Output Voltage (Referenced to GND)                                                                 | 0           | V <sub>CC</sub>    | V    |
| T <sub>A</sub>                     | Operating Temperature, All Package Types                                                                             | -55         | +125               | °C   |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time (Figure 1)<br>V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.



**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions                                                                                                                    | V <sub>CC</sub><br>V | Guaranteed Limit     |                    |                    | Unit |
|-----------------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|--------------------|--------------------|------|
|                 |                                                |                                                                                                                                    |                      | 25 °C<br>to<br>-55°C | ≤85<br>°C          | ≤125<br>°C         |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V<br>  I <sub>OUT</sub>   ≤ 20 µA                                                  | 2.0<br>4.5<br>6.0    | 1.5<br>3.15<br>4.2   | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| V <sub>IL</sub> | Maximum Low -Level Input Voltage               | V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V<br>  I <sub>OUT</sub>   ≤ 20 µA                                                  | 2.0<br>4.5<br>6.0    | 0.5<br>1.35<br>1.8   | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>  I <sub>OUT</sub>   ≤ 20 µA                                                | 2.0<br>4.5<br>6.0    | 1.9<br>4.4<br>5.9    | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
|                 |                                                | V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>  I <sub>OUT</sub>   ≤ 6.0 mA<br>  I <sub>OUT</sub>   ≤ 7.8 mA              | 4.5<br>6.0           | 3.98<br>5.48         | 3.84<br>5.34       | 3.7<br>5.2         |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>  I <sub>OUT</sub>   ≤ 20 µA                                               | 2.0<br>4.5<br>6.0    | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|                 |                                                | V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>  I <sub>OUT</sub>   ≤ 6.0 mA<br>  I <sub>OUT</sub>   ≤ 7.8 mA             | 4.5<br>6.0           | 0.26<br>0.26         | 0.33<br>0.33       | 0.4<br>0.4         |      |
| I <sub>IN</sub> | Maximum Input Leakage Current                  | V <sub>IN</sub> =V <sub>CC</sub> or GND                                                                                            | 6.0                  | ±0.1                 | ±1.0               | ±1.0               | µA   |
| I <sub>OZ</sub> | Maximum Three State Leakage Current            | Output in High-Impedance State<br>V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub><br>V <sub>OUT</sub> = V <sub>CC</sub> or GND | 6.0                  | ±0.5                 | ±5.0               | ±10                | µA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>IN</sub> =V <sub>CC</sub> or GND<br>I <sub>OUT</sub> =0µA                                                                   | 6.0                  | 4.0                  | 40                 | 160                | µA   |

# SL74HC573

## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

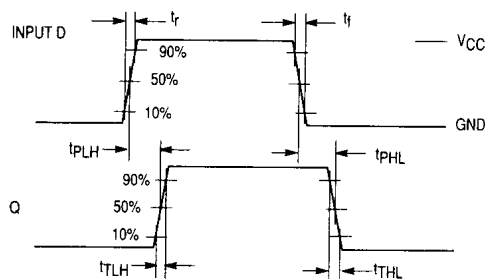
| Symbol                              | Parameter                                                                  | V <sub>CC</sub><br>V | Guaranteed Limit  |       |        | Unit |
|-------------------------------------|----------------------------------------------------------------------------|----------------------|-------------------|-------|--------|------|
|                                     |                                                                            |                      | 25 °C to<br>-55°C | ≤85°C | ≤125°C |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Maximum Propagation Delay, Input D to Q<br>(Figures 1 and 5)               | 2.0                  | 150               | 190   | 225    | ns   |
|                                     |                                                                            | 4.5                  | 30                | 38    | 45     |      |
|                                     |                                                                            | 6.0                  | 26                | 33    | 38     |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Maximum Propagation Delay, Latch Enable<br>to Q (Figures 2 and 5)          | 2.0                  | 160               | 200   | 240    | ns   |
|                                     |                                                                            | 4.5                  | 32                | 40    | 48     |      |
|                                     |                                                                            | 6.0                  | 27                | 34    | 41     |      |
| t <sub>PLZ</sub> , t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Q<br>(Figures 3 and 6)         | 2.0                  | 150               | 190   | 225    | ns   |
|                                     |                                                                            | 4.5                  | 30                | 38    | 45     |      |
|                                     |                                                                            | 6.0                  | 26                | 33    | 38     |      |
| t <sub>PZH</sub> , t <sub>PZL</sub> | Maximum Propagation Delay, Output Enable to Q<br>(Figures 3 and 6)         | 2.0                  | 150               | 190   | 225    | ns   |
|                                     |                                                                            | 4.5                  | 30                | 38    | 45     |      |
|                                     |                                                                            | 6.0                  | 26                | 33    | 38     |      |
| t <sub>TLH</sub> , t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 5)            | 2.0                  | 60                | 75    | 90     | ns   |
|                                     |                                                                            | 4.5                  | 12                | 15    | 18     |      |
|                                     |                                                                            | 6.0                  | 10                | 13    | 15     |      |
| C <sub>IN</sub>                     | Maximum Input Capacitance                                                  | -                    | 10                | 10    | 10     | pF   |
| C <sub>OUT</sub>                    | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State) | -                    | 15                | 15    | 15     | pF   |

|                 |                                                                                                                                                         |                                      |    |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Enabled Output)                                                                                                      | Typical @25°C,V <sub>CC</sub> =5.0 V | pF |
|                 | Used to determine the no-load dynamic power consumption: P <sub>D</sub> =C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f+I <sub>CC</sub> V <sub>CC</sub> | 23                                   |    |

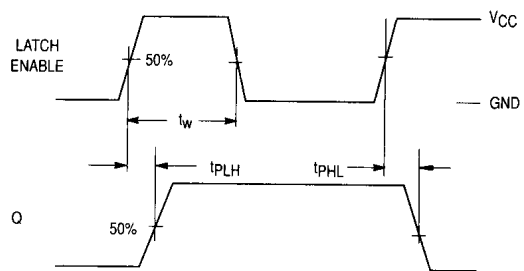
## TIMING REQUIREMENTS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

| Symbol                          | Parameter                                                    | V <sub>CC</sub><br>V | Guaranteed Limit  |       |        | Unit |
|---------------------------------|--------------------------------------------------------------|----------------------|-------------------|-------|--------|------|
|                                 |                                                              |                      | 25 °C to<br>-55°C | ≤85°C | ≤125°C |      |
| t <sub>SU</sub>                 | Minimum Setup Time, Input D<br>to Latch Enable<br>(Figure 4) | 2.0                  | 50                | 65    | 75     | ns   |
|                                 |                                                              | 4.5                  | 10                | 13    | 15     |      |
|                                 |                                                              | 6.0                  | 9                 | 11    | 13     |      |
| t <sub>H</sub>                  | Minimum Hold Time, Latch<br>Enable to Input D<br>(Figure 4)  | 2.0                  | 5                 | 5     | 5      | ns   |
|                                 |                                                              | 4.5                  | 5                 | 5     | 5      |      |
|                                 |                                                              | 6.0                  | 5                 | 5     | 5      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Latch<br>Enable (Figure 2)              | 2.0                  | 75                | 95    | 110    | ns   |
|                                 |                                                              | 4.5                  | 15                | 19    | 22     |      |
|                                 |                                                              | 6.0                  | 13                | 16    | 19     |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall<br>Times (Figure 1)              | 2.0                  | 1000              | 1000  | 1000   | ns   |
|                                 |                                                              | 4.5                  | 500               | 500   | 500    |      |
|                                 |                                                              | 6.0                  | 400               | 400   | 400    |      |

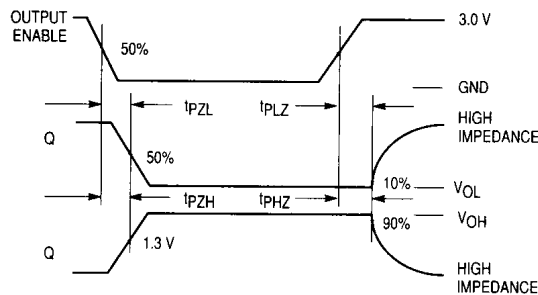




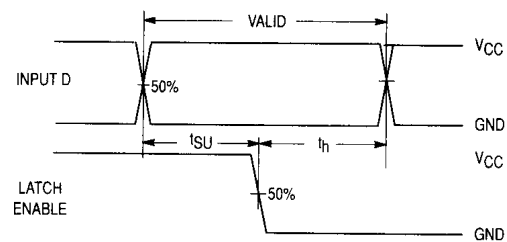
**Figure 1. Switching Waveforms**



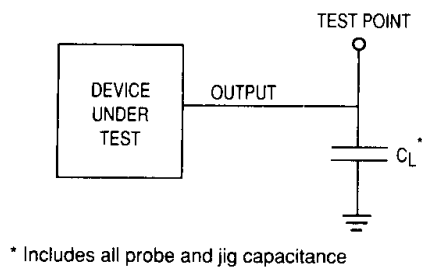
**Figure 2. Switching Waveforms**



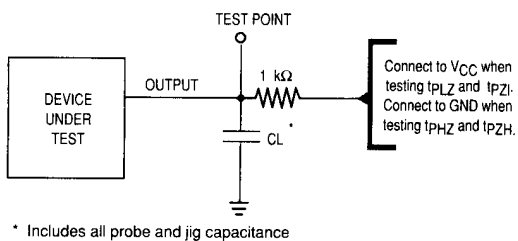
**Figure 3. Switching Waveforms**



**Figure 4. Switching Waveforms**



**Figure 5. Test Circuit**



**Figure 6. Test Circuit**

## EXPANDED LOGIC DIAGRAM

