

## DUAL 4-BIT BINARY RIPPLE COUNTER

## FEATURES

- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Output capability: standard
- I<sup>2</sup>C category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT393 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT393 are 4-bit binary ripple counters with separate clocks ( $1\overline{CP}$  and  $2\overline{CP}$ ) and master reset ( $1MR$  and  $2MR$ ) inputs to each counter. The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description. A HIGH level on the  $nMR$  input overrides the clock and sets the outputs LOW.

| SYMBOL            | PARAMETER                                                                                | CONDITIONS                                    | TYPICAL       |               | UNIT           |
|-------------------|------------------------------------------------------------------------------------------|-----------------------------------------------|---------------|---------------|----------------|
|                   |                                                                                          |                                               | HC            | HCT           |                |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>$n\overline{CP}$ to $nQ_0$<br>$nQ$ to $nQ_{n+1}$<br>$nMR$ to $nQ_n$ | $C_L = 15\text{ pF}$<br>$V_{CC} = 5\text{ V}$ | 12<br>5<br>11 | 20<br>6<br>15 | ns<br>ns<br>ns |
| $f_{max}$         | maximum clock frequency                                                                  |                                               | 99            | 53            | MHz            |
| $C_I$             | input capacitance                                                                        |                                               | 3.5           | 3.5           | pF             |
| $CPD$             | power dissipation<br>capacitance per counter                                             | notes 1 and 2                                 | 23            | 25            | pF             |

$GND = 0\text{ V}$ ;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

## Notes

1.  $CPD$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
 For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5\text{ V}$

## PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).

14-lead mini-pack; plastic (SO14; SOT108A).

## PIN DESCRIPTION

| PIN NO.                     | SYMBOL                                 | NAME AND FUNCTION                              |
|-----------------------------|----------------------------------------|------------------------------------------------|
| 1, 13                       | $1\overline{CP}$ , $2\overline{CP}$    | clock inputs (HIGH-to-LOW, edge-triggered)     |
| 2, 12                       | $1MR$ , $2MR$                          | asynchronous master reset inputs (active HIGH) |
| 3, 4, 5, 6,<br>11, 10, 9, 8 | $1Q_0$ to $1Q_3$ ,<br>$2Q_0$ to $2Q_3$ | flip-flop outputs                              |
| 7                           | GND                                    | ground (0 V)                                   |
| 14                          | $V_{CC}$                               | positive supply voltage                        |

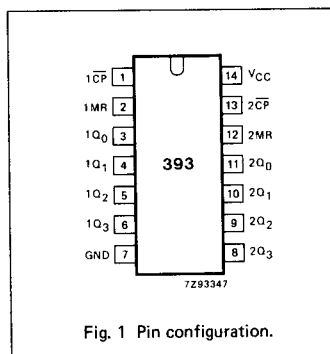


Fig. 1 Pin configuration.

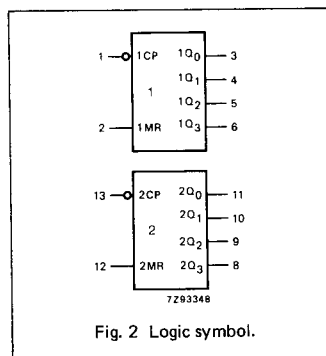


Fig. 2 Logic symbol.

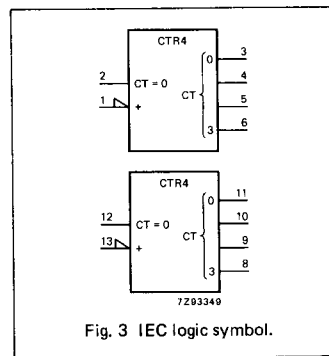
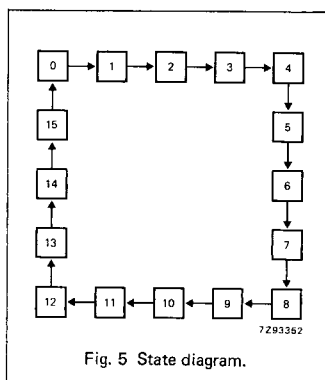
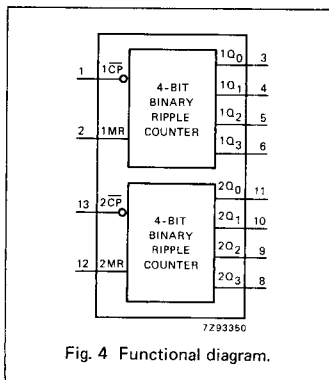


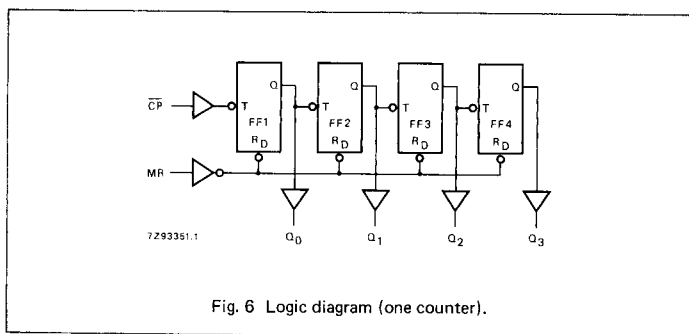
Fig. 3 IEC logic symbol.



COUNT SEQUENCE FOR 1 COUNTER

| COUNT | OUTPUTS        |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| 0     | L              | L              | L              | L              |
| 1     | H              | L              | L              | L              |
| 2     | L              | H              | L              | L              |
| 3     | L              | L              | H              | L              |
| 4     | L              | L              | L              | H              |
| 5     | H              | L              | L              | H              |
| 6     | L              | H              | L              | H              |
| 7     | L              | L              | H              | H              |
| 8     | L              | L              | L              | H              |
| 9     | H              | L              | L              | H              |
| 10    | L              | H              | L              | H              |
| 11    | L              | L              | H              | H              |
| 12    | L              | L              | H              | H              |
| 13    | H              | L              | H              | H              |
| 14    | L              | H              | H              | H              |
| 15    | H              | H              | H              | H              |

H = HIGH voltage level  
L = LOW voltage level



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

GND = 0 V;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$

| SYMBOL                                 | PARAMETER                                                 | T <sub>amb</sub> (°C) |                 |                 |                 |                 |                 | UNIT            | TEST CONDITIONS      |                   |        |
|----------------------------------------|-----------------------------------------------------------|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------------|-------------------|--------|
|                                        |                                                           | 74HC                  |                 |                 |                 |                 |                 |                 | V <sub>CC</sub><br>V | WAVEFORMS         |        |
|                                        |                                                           | +25                   |                 |                 | −40 to +85      |                 | −40 to +125     |                 |                      |                   |        |
|                                        |                                                           | min.                  | typ.            | max.            | min.            | max.            | min.            |                 |                      |                   | max.   |
| t <sub>PHL</sub> /<br>t <sub>PLH</sub> | propagation delay<br>nCP to nQ <sub>0</sub>               |                       | 41<br>15<br>12  | 125<br>25<br>21 |                 | 155<br>31<br>26 |                 | 190<br>38<br>32 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 7 |
| t <sub>PHL</sub> /<br>t <sub>PLH</sub> | propagation delay<br>nQ <sub>n</sub> to nQ <sub>n+1</sub> |                       | 14<br>5<br>4    | 45<br>9<br>8    |                 | 55<br>11<br>9   |                 | 70<br>14<br>12  | ns                   | 2.0<br>4.5<br>6.0 | Fig. 7 |
| t <sub>PHL</sub>                       | propagation delay<br>nMR to nQ <sub>n</sub>               |                       | 39<br>14<br>11  | 140<br>28<br>24 |                 | 175<br>35<br>30 |                 | 210<br>42<br>36 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 8 |
| t <sub>THL</sub> /<br>t <sub>TLH</sub> | output transition time                                    |                       | 19<br>7<br>6    | 75<br>15<br>13  |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 7 |
| t <sub>W</sub>                         | clock pulse width<br>HIGH or LOW                          | 80<br>16<br>14        | 17<br>6<br>5    |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 7 |
| t <sub>W</sub>                         | master reset pulse<br>width; HIGH                         | 80<br>16<br>14        | 19<br>7<br>6    |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 8 |
| t <sub>rem</sub>                       | removal time<br>nMR to nCP                                | 5<br>5<br>5           | 3<br>1<br>1     |                 | 5<br>5<br>5     |                 | 5<br>5<br>5     |                 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 8 |
| f <sub>max</sub>                       | maximum clock pulse<br>frequency                          | 6<br>30<br>35         | 30<br>90<br>107 |                 | 5<br>24<br>28   |                 | 4<br>20<br>24   |                 | MHz                  | 2.0<br>4.5<br>6.0 | Fig. 7 |

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-------|-----------------------|
| 1CP   | 0.4                   |
| 2CP   | 0.4                   |
| 1MR   | 1.0                   |
| 2MR   | 1.0                   |

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                                 | PARAMETER                                                 | T <sub>amb</sub> (°C) |      |      |            |      |             | UNIT | TEST CONDITIONS      |           |        |
|----------------------------------------|-----------------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|----------------------|-----------|--------|
|                                        |                                                           | 74HCT                 |      |      |            |      |             |      | V <sub>CC</sub><br>V | WAVEFORMS |        |
|                                        |                                                           | +25                   |      |      | -40 to +85 |      | -40 to +125 |      |                      |           |        |
|                                        |                                                           | min.                  | typ. | max. | min.       | max. | min.        |      |                      |           | max.   |
| t <sub>PHL</sub> /<br>t <sub>PLH</sub> | propagation delay<br>nCP to nQ <sub>0</sub>               |                       | 15   | 25   |            | 31   |             | 38   | ns                   | 4.5       | Fig. 7 |
| t <sub>PHL</sub> /<br>t <sub>PLH</sub> | propagation delay<br>nQ <sub>n</sub> to nQ <sub>n+1</sub> |                       | 6    | 10   |            | 13   |             | 15   | ns                   | 4.5       | Fig. 7 |
| t <sub>PHL</sub>                       | propagation delay<br>nMR to nQ <sub>n</sub>               |                       | 18   | 32   |            | 40   |             | 48   | ns                   | 4.5       | Fig. 8 |
| t <sub>THL</sub> /<br>t <sub>TLH</sub> | output transition time                                    |                       | 7    | 15   |            | 19   |             | 22   | ns                   | 4.5       | Fig. 7 |
| t <sub>W</sub>                         | clock pulse width<br>HIGH or LOW                          | 19                    | 11   |      | 24         |      | 29          |      | ns                   | 4.5       | Fig. 7 |
| t <sub>W</sub>                         | master reset pulse<br>width; HIGH                         | 16                    | 6    |      | 20         |      | 24          |      | ns                   | 4.5       | Fig. 8 |
| t <sub>rem</sub>                       | removal time<br>nMR to nCP                                | 5                     | 0    |      | 5          |      | 5           |      | ns                   | 4.5       | Fig. 8 |
| f <sub>max</sub>                       | maximum clock pulse<br>frequency                          | 27                    | 48   |      | 22         |      | 18          |      | MHz                  | 4.5       | Fig. 7 |

## AC WAVEFORMS

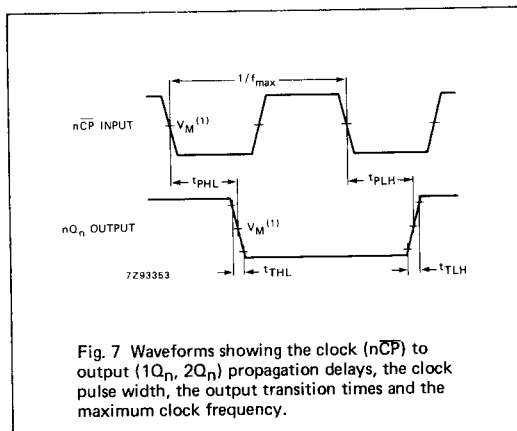


Fig. 7 Waveforms showing the clock ( $\overline{nCP}$ ) to output ( $1Q_n$ ,  $2Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

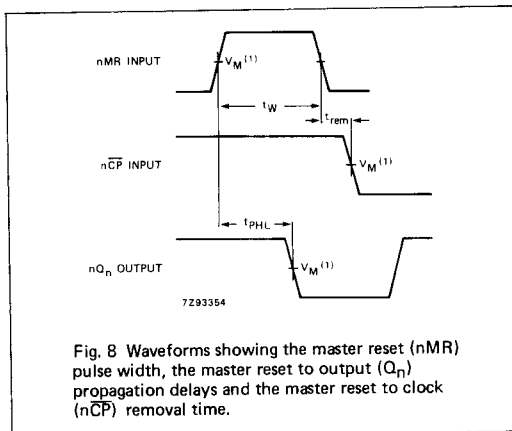


Fig. 8 Waveforms showing the master reset ( $\overline{nMR}$ ) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock ( $\overline{nCP}$ ) removal time.

## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .